| SIES Graduate School of Technology (Autonomous) NAAC A+ (Affiliated to University of Mumbai) | ***End Semester Examination (R-24) SH 2025 Answer Key with marking scheme*** |
|---|---|
| Branch: Computer Engineering/AIDS/AIML | Course: Computer Organization and Architecture |
| Year/ Semester: SE/III | Course code: CEC305/AIDSC305/AIMLC305 |
| Time: 02 hours | Marks: 60 |

| | | Marks |
|---|---|---|
| Q. 1 | Attempt any FOUR. (All questions carry equal marks) | **15** |
| A. | • Definition of CO and CA – **1 mark**<br>-CO deals with hardware implementation and functional units, while CA deals with attributes visible to the programmer.<br>• At least 3 parameters – **2 marks**<br>• Differentiation (tabular) – **2 marks** | 5 |
| B. | • Listing all modes – **1 mark**<br>Mode 0: Simple I/O<br>Mode 1: Handshake I/O<br>Mode 2: Bidirectional I/O<br>BSR: Bit Set Reset control for Port C.<br>• Explanation of each mode – **3 marks**<br>• Mention of BSR mode – **1 mark** | 5 |
| C. | • Definition – **1 mark**<br>-Addressing mode defines how operands are accessed.<br>• Each addressing mode explanation with example – **2 marks** each<br>Examples:<br>• Immediate (MOV A, #05H)<br>• Direct (MOV A, 30H)<br>• Indirect, Register, Indexed (any two expected). | 5 |
| D. | • Concept – **1 mark**<br>-Multi-core contains multiple processing units within one chip.<br>-Enhances parallel execution, multitasking, and throughput.<br>-Example: Dual-core, Quad-core systems.<br>• Working and architecture – **2 marks**<br>• Performance improvement explanation – **2 marks** | 5 |
| | | 5 |
| Q.2 | | **30** |
| A. | • Binary representation and 2's complement – **3 marks**<br>• Stepwise Booth's algorithm operations – **5 marks**<br>• Final result with verification – **2 marks** | 10 |

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| B. | • Neat labeled diagram – **4 marks**<br>• Explanation of BIU and EU – **4 marks**<br>• Functional units overview – **2 marks**<br>**Expected Points:**<br>BIU: Instruction queue, segment registers, bus interface.<br>EU: ALU, control unit, flag register.<br>Mention pipelining and segmented memory model. | 10 |
| C. | • Concept of virtual memory – **3 marks**<br>• Paging explanation – **3 marks**<br>• Segmentation explanation – **3 marks**<br>• Diagram/summary **– 1 mark**<br>**Expected Points:**<br>• Virtual memory extends logical memory beyond physical.<br>• Paging: Fixed-size blocks using page tables<br>• Segmentation: Logical division into code, data, stack segments. | 10 |
| D. | • Calculation of main memory bits – **3 marks**<br>• Calculation of set, tag, and word fields – **6 marks**<br>• Final answers – **1 mark**<br>SET =4 bits, TAG=8bits, Word=7 bits | 10 |
| E. | • Definition – **2 marks**<br>• Explanation of microprogram control – **2 marks**<br>• Microinstruction sequence for MOV – **3 marks**<br>• Microinstruction sequence for ADD – **3 marks**<br>**Solution:**<br>**Micro-operations**<br>1)MAR=PC; PCout, MARin, RD<br>LOAD MDR from memory; PCin, MDRinE, WMFC<br>PC=PC+1<br>IR=MDR;MDRout, IRin<br>R3=R4; R4out, R3in<br><br>**Micro-operations**<br>2) MAR=PC; PCout, MARin, RD<br>LOAD MDR from memory; PCin, MDRinE, WMFC<br>PC=PC+1<br>IR=MDR; MDRout, IRin<br>Y=R3; R3out,Yin<br>R4out, Select Y, Add, Zin<br>Zout, R3in | 10 |
| | | |
| Q.3 | | **15** |

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|---|---|---|
| A. | • Neat labelled diagram – **2 marks**<br>• Explanation of each block – **3 marks**<br>-Include Input, Output, Memory, ALU, and Control Unit.<br>-Explain data and control flow between units | 5 |
| B. | • Concept – **1 mark**<br>• Working principle – **2 marks**<br>• Advantages and limitations – **2 marks**<br>**Expected Points:**<br>Uses fixed logic circuits for control.<br>Fast operation but lacks flexibility.<br>Implemented using combinational logic. | 5 |
| C. | • Meaning of BSR mode – **1 mark**<br>• Control word format – **3 marks**<br>• Explanation of bits – **1 mark**<br>**Expected Points:**<br>D7 = 0 for BSR mode.<br>D3–D1 select bit of Port C.<br>D0 determines Set (1) or Reset (0). | 5 |
| D. | • Definition/classification basis – **1 mark**<br>• Explanation of 4 types – **3 marks**<br>• Example – **1 mark**<br>**Expected Points:**<br>Classification based on instruction and data streams.<br>SISD, SIMD, MISD, MIMD.<br>Examples: SISD (single CPU), SIMD (vector processors), MIMD (multicore). | 5 |