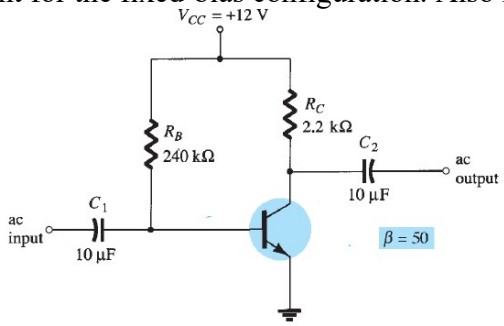
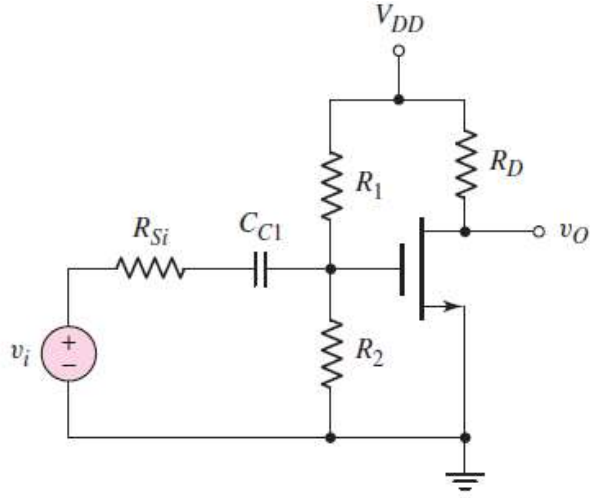
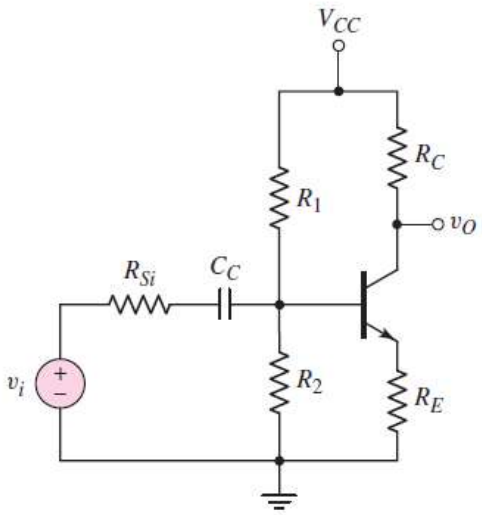
(Affiliated to University of Mumbai)	***End Semester Examination (R-24)SH 2025 Answer Key with marking scheme***
Branch: EXTC	Course: Electronic Devices and Circuit
Year/ Semester: SE/ III	Course code:ETC 302
Time: 03 hours	Marks: 80

		Marks
Q. 1	Attempt any FOUR. (All questions carry equal marks)	
A.	Diagram of CE-CE multistage amplifier---- 3 Marks Comment on its voltage gain… 2Marks	5
B.	Differentiate small signal and Large signal amplifier ---- Any 7 Point	5
C.	Diagram --- 1 Mark working principle of Zener diode---2 Mark characteristics and applications.--- 2 Marks	5
D.	Q point for the fixed-bias configuration. Also Determine V_b and V_c  . $I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$ $I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$ $V_{CE_Q} = V_{CC} - I_C R_C$ $= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$ $= \mathbf{6.83\ V}$ $V_B = V_{BE} = \mathbf{0.7\ V}$ $V_C = V_{CE} = \mathbf{6.83\ V}$	5
E.	Region of operation of MOSFET Diagram : 2 Marks Explanation: 3 Marks	5
F.	Statement of Miller Theorem : 2.5 Marks Explanation Miller's Theorem: 2.5 Marks	5
Q.2	Attempt any FOUR. (All questions carry equal marks)	
A.	N-channel JFET. Construction : 3 Marks Working : 4 Marks	10 Marks

	Characteristics : 3 Marks	
B.	Expression for the small-signal voltage gain and input resistance of common-emitter circuit with an emitter resistor. Diagram basic circuit : 2 Marks Equivalent Hybrid Pi model : 2 Marks Derivation : 6 Marks	10
C.	Small-signal voltage gain and input of a common-source amplifier. The parameters are: VDD = 3.3 V, RD = 10 k, $R1$ = 140 k, $R2$ = 60 k, and RSi = 4 k. The transistor parameters are: VTN = 0.4 V, Kn = 0.5 mA/V2, and λ = 0.02 V−1. 	10

	Solution (dc calculations): The dc or quiescent gate-to-source voltage is $$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{60}{140 + 60}\right)(3.3) = 0.99\,\text{V}$$ The quiescent drain current is $$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2 = (0.5)(0.99 - 0.4)^2 = 0.174\,\text{mA}$$ and the quiescent drain-to-source voltage is $$V_{DSQ} = V_{DD} - I_{DQ}R_D = 3.3 - (0.174)(10) = 1.56\,\text{V}$$ Since $V_{DSQ} > V_{GSQ} - V_{TN}$, the transistor is biased in the saturation reg **Small-signal Voltage Gain:** The small-signal transconductance g_m is then $$g_m = 2\sqrt{K_n I_{DQ}} = 2\sqrt{(0.5)(0.174)} = 0.590\,\text{mA/V}$$ and the small-signal output resistance is $$r_o = \frac{1}{\lambda I_Q} = \frac{1}{(0.02)(0.174)} = 287\,\text{k}\Omega$$ The input resistance to the amplifier is $$R_i = R_1 \| R_2 = 140 \| 60 = 42\,\text{k}\Omega$$ From Figure 4.15 and Equation (4.29), the small-signal voltage gain is $$A_v = -g_m(r_o \| R_D)\left(\frac{R_i}{R_i + R_{Si}}\right) = -(0.59)(287 \| 10)\left(\frac{42}{42 + 4}\right)$$ or $$A_v = -5.21$$	
D.	Draw and explain high frequency model for BJT in CE configuration Diagram High Frequency model : 4 Marks Explanation : 6 Marks	5
E.	Expression for Zi, Zo and AV for CS E- MOSFET amplifier using hybrid pi model Diagram basic circuit : 2 Marks Equivalent Hybrid Pi model : 2 Marks Derivation : 6 Marks	5
F.	Corner frequency and maximum gain of a bipolar common emitter Circuit with a coupling capacitor. The parameters are: $R1$ = 51.2 k,$R2$ = 9.6 k_, RC = 2 k_, RE = 0.4 k, RSi = 0.1 k_, CC = 1 μF, and VCC =10 V. The transistor parameters are: VBE(on) = 0.7 V, β = 100, and VA =∞.	5



Solution: From a dc analysis, the quiescent collector current is $I_{CQ} = 1.81$ mA. The small-signal parameters are $g_m = 69.6$ mA/V and $r_\pi = 1.44\,\text{k}\Omega$.

The input resistance is

$$R_i = R_1 \| R_2 \| [r_\pi + (1+\beta)R_E]$$
$$= 51.2 \| 9.6 \| [1.44 + (101)(0.4)] = 6.77\,\text{k}\Omega$$

and the time constant is therefore

$$\tau_S = (R_{Si} + R_i)C_C = (0.1 \times 10^3 + 6.77 \times 10^3)(1 \times 10^{-6}) \Rightarrow 6.87\ \text{ms}$$

The corner frequency is

$$f_L = \frac{1}{2\pi\tau_S} = \frac{1}{2\pi(6.87 \times 10^{-3})} = 23.2\,\text{Hz}$$

Finally, the maximum voltage gain magnitude is

$$|A_v|_{\max} = \frac{g_m r_\pi R_C}{(R_{Si} + R_i)}\left(\frac{R_B}{R_B + R_{ib}}\right)$$

where

$$R_{ib} = r_\pi + (1+\beta)R_E = 1.44 + (101)(0.4) = 41.8\,\text{k}\Omega$$

Q.3	Attempt any FOUR	**5**
A.	Diagram : 1 Mark Characteristics : 1 Mark Explanation : 3 marks	5
B.	Need of biasing circuits---- 3 Marks list different biasing circuits for BJT---- 2 Marks	5
C.	Explanation effect of coupling capacitor on frequency response of a single stage CE amplifier… 2.5 Marks . effect of bypass capacitor on frequency response of a single stage CE amplifier…	5

	2.5 Marks .	
D.	Explain concept of multistage amplifier.---2.5 Marks State its advantage and Disadvantage.--- 2.5 Marks	5
E.	cross over distortion in Class B power amplifier. Graph : 2 Marks Explanation : 3 Marks	5
F.	Draw Voltage divider circuit for E MOSFET. Derive Q point expression for same. Circuit Diagram : 2 Marks Derivation : 3 Marks	5