(Affiliated to University of Mumbai)	***End Semester Examination (R-24/R-25) SH 2026 Answer Key with marking scheme***
Branch: EXTC	Course: Microprocessor and Microcontroller
Year/ Semester: SE/ III	Course code:ETC 303
Time: 03 hours	Marks: 80

		Marks
Q. 1	All questions are compulsory.	

A.	• 8086 has a **20-bit physical address bus** and can address **1 MB memory**. **[1]**
	• Memory is divided into four logical segments:
	  • **Code Segment (CS)** – stores program instructions.
	  • **Data Segment (DS)** – stores data.
	  • **Stack Segment (SS)** – stores stack data.
	  • **Extra Segment (ES)** – additional data segment. **[2]**
	• Physical address is calculated as:
	Physical Address = Segment × 10H + Offset
	Example: If **CS = 2000H** and **IP = 1234H**,
	Physical Address = 2000H × 10H + 1234H = 21234H. **[2]**
		05

B.	1 mark for each correctly explained mode with example. 5 addressing mode	05
C.	Any five relevant features, **1 mark each**:	05
D.	• **TCON (Timer/Counter Control) register** is an 8-bit register used to control timers and monitor external interrupts. **[2]** **Bit Name Function** 7 TF1 Timer 1 overflow flag 6 TR1 Timer 1 run control 5 TF0 Timer 0 overflow flag 4 TR0 Timer 0 run control 3 IE1 External interrupt 1 flag 2 IT1 Interrupt 1 type control 1 IE0 External interrupt 0 flag 0 IT0 Interrupt 0 type control • **TF1, TF0:** Set when the respective timer overflows. **[1]** • **TR1, TR0:** Start/stop Timer 1 and Timer 0. **[1]** • **IE1, IE0:** Indicate external interrupt requests. **[0.5]** • **IT1, IT0:** Select edge-triggered or level-triggered external interrupts. **[0.5]**	05

E.	• Assembler directives provide instructions to the assembler for organizing and defining the program; they are not executed by the microcontroller. **[1]**
	
	Any four with suitable examples, **1 mark each**:
	
	• **ORG** – specifies starting address
	`ORG 0000H`
	• **END** – indicates end of source program
	`END`
	• **DB** – defines byte data
	`MSG: DB 'HELLO'`
	• **EQU** – assigns a symbolic constant
	`COUNT EQU 05H`
	• **DW** – defines a word
	`DATA DW 1234H`
		05

F.	• Diagram –2 Marks Explanation – 3Marks	05
Q.2A	Diagram : 4 Marks Explanation : 6Marks	10
Q.2B.	• Types/sources of interrupts in 8086 – **2 marks** • Interrupt Vector Table (IVT) organization – **2 marks** • Role of interrupt vector and vector address – **2 marks** • Interrupt servicing sequence – **3 marks** • Return from ISR using `IRET` – **1 mark**	10
Q.3A	Diagram : 4 Marks Explanation : 6Marks	10
Q.3B	Integer pipeline Explanation : 5 Marks Floating Point Pipeline Explanation : 5 Marks	10
Q.4A	• Initial value calculation – **2** Marks • TMOD, TH1 and TL1 initialization – **1Marks** • Assembly program with comment – **6 marks** **Assumption:** Crystal frequency = **11.0592 MHz**	
	OR	
Q.4B	SCON value : 2 Marks TMOD value : 2 Marks Program with comment : 6 Marks	10
Q.5A	• Interrupt sources – **2.5** Marks • Explanation – **2** Marks • Interrupt flags – **1.5** Marks • IE register – **1** Mark	10

	• IP register – **1** Mark Interrupt priority – **2 Mark**	
	OR	
Q.5B	• Neat memory organization diagram – **2 marks** • Program/code memory organization explanation – **3 marks** • Internal data RAM organization explanation – **2 marks** • SFR space explanation – **1 mark** • Register banks/bit-addressable area explanation – **2 marks**	10
Q.6A	• Neat programmer's model/register diagram – **3 marks** • R0–R12 general-purpose registers – **2 marks** • SP (R13), LR (R14) and PC (R15) – **3 marks** • CPSR and its function – **2 marks**	10
	OR	
Q.6B	7 interrupt : 7 Marks Interrupt handling sequence : 3 Marks	10
	*********** All the Best***********	