(Affiliated to University of Mumbai)	***End Semester Examination (R-24) SH 2025 Answer Key with marking scheme***
Branch: IT	Course: Computer Organization and Architecture
Year/ Semester: II/III	Course code: ITC305
Time: 03 hours	Marks: 80

		Marks
Q. 1	Attempt any FOUR. (All questions carry equal marks)	
A.	Von Neumann architecture Explanation Diagram	 03 02
B.	ROL & RCR instructions of 8086 microprocessors Explanation of both the instructions Example of each	 03 02
C.	Difference between Hardwired and Micro programmed control unit 5 points of differences	 05
D.	flowchart of unsigned binary restoring division algorithm Explanation	02 03
E.	Speed, accuracy, size, cost, access time, access mode, volatility 5 points explanation	05
F.	Processor Communication, Control and Timing, Data Buffering, Error Detection, Device Communication explanation	 05
Q.2	Attempt any FOUR. (All questions carry equal marks)	
A.	architecture of 8086 diagram Explanation	 04 06
B.	addressing modes of 8086 microprocessor Names, Description Example	 05 05
C.	Flynn's classification Diagram Explanation of diagram	 05 05
D.	non restoring division algorithm to divide 14 by 3. Conversion of 14 & 3 in binary 4 Iterations Answer	 01 08 01
E.	cache memory mapping techniques Diagram Explanation	 04 06
F.	Associative memory Diagram Working with explanation	04 06
Q.3	Attempt any FOUR. (All questions carry equal marks)	
A.	Computer Organization and Computer Architecture 3 to 4 points of comparison	 05
B.	Ready signal function INTR signal function	2.5 2.5
C.	5 points of differences between Procedure & Macros	05
D.	nano programming Diagram	02

	Explanation	03
E.	Booth's algorithm flowchart Explanation	03 02
F.	functions of 8089 I/O processor with explanation	05