**SIES Graduate School of Technology**

**Department Of Electronics and Telecommunication Engineering**

# Workshop on Digital System Design on FPGA Using Verilog

**15th January 2025 to 15th February 2025**
**Click here to register**

Since their introduction in the 1985, field programmable gate arrays (FPGAs) have become increasingly important to the electronics industry. They have the potential for higher performance and lower power consumption than microprocessors and compared with ASICs, offer lower non-recurrent engineering (NRE) costs, reduced development time, easier debugging and reduced risk. Since modern FPGAs can meet many of the performance requirements of ASICs, they are being increasingly used in their place. The aim of workshop is to provide a platform for students to learn, design and implement digital system on FPGA using Verilog/VHDL.

In this course students will learn Basics of FPGA Board , FPGA Programming using Verilog.

## About Instructors:

This course will be taught by a team of expert from SIESGST faculty-Electronics and Telecommunication Department, along with some Industry Experts.

**Faculty Members:**

1. Prof. Dr.PreetiHemnani
2. Prof. Pranavi Nikam

## CourseObjectives:

| |
|---|
| • To undersatnd FPGA and HDL language |
| • To understand design of combinational circuit using verilog |
| • To understand design of sequential circuit using verilog |
| • To understand Test bench and simulation uisng different tools |
| • To understand Finite state mahine design using verilog |
| • To undersatnd FPGA and HDL language |

## Course Outcomes:

At the end of the course, students will be able to

| |
|---|
| • Implement Verilog design using EDA and xilink platform |
| • Implement combinational circuits using Verilog |
| • Implement sequential circuits using Verilog |
| • Implement FSM using Verilog |
| • Implement hamming code , error detetction and correction using verilog |

## CourseContent:

| Module | Contents | Hours |
|---|---|---|
| 1. | 1.1 Introduction to basics of FPGA<br>1.2 Introduction to Verilog coding: Data types , Constant, Parameters, Wires , Registers , operators | 4hrs |
| 2. | 2.1 Continues and Procedural assignment statement<br>2.2 Different Modeling style : Gate level, Structural level, Behavioral Level<br>2.3 Programming based on different modeling style<br>2.4 Xilink software introduction | 7hrs |
| 3. | 3.1: Implementation of combinational circuits on FPGA: Half adder , Full adder , Multiplexer, Decoder | 6hrs |
| 4 | 4.1 : Implementation of sequential circuits on FPGA<br>Flip Flop, Asynchronous counter, Synchronous counter, Mod counter , Sequence detector | 8 hrs |
| 5 | 5.1 : FSM design<br>5.2: FSM implementation on FPGA | 2hrs<br>6 hrs |
| 6 | Hamming code, Error detetction and correction using verilog on FPGA | 6 Hrs |
| 7 | Designing of Projects . | 15hrs |

## Assessment:

1. Module wise assignments and quizzes will be taken.
2. Mini Projects will be assigned in a group of 4 students.

## CourseCoordinators:

Dr. Preeti Hemnani

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Pranavi Nikam

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9870201503

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Sri Chandrasekarendra Saraswati Vidyapuram
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**Department of Electronics & Telecommunication Engineering**

# Event Report

## Digital System Design on FPGA using Verilog
**(15/1/2025 to 15/2/2025)**

| Event Information |
|---|
| **Event Type:** Student Development program with Intenship |
| **Event title**: Digital System Design on FPGA using Verilog |
| **Resource Person:** Dr.Preeti Hemnani , Prof. Pranavi Nikam |
| **Event date:15/1/2025 to 15/2/2025** |
| **Organized for:**Student Faculty ☐ |
| **Organizedby** Department : Electronics & Telecommunication Engineering |
| **Target audience :TE students**<br>**Branch: EXTC**<br>**Number of students registered:31**<br>**Number of students joined on first day:31**<br>**Number of students completed the course:31**<br>**Number of students completed the internship projects:31** |
| **Attachments: 1. List of students with internship Projects completed by the students**<br>**2. Attendance report**<br>**3. Feedback**<br>**4. Certificate, Photographs (in JPEG/PNG)** |

## Event Description

EXTC department faculties have conducted 1 month student development program on “Digital System Design on FPGA using Verilog” followed by internship and projects. Program was conducted by Prof. Pranavi Nikam and Prof. Dr. Preeti Hemnani.

Objective of the workshop was to bridge the gap between industry requirements and academic. 31 students attended the course and successfully developed and submitted project .
Students completed their projects during online internship by SIESGST.

Certificates were given to students on successful completion and presentation of developed applications. Feedback was collected and overall feedback shows students were satisfied with content.

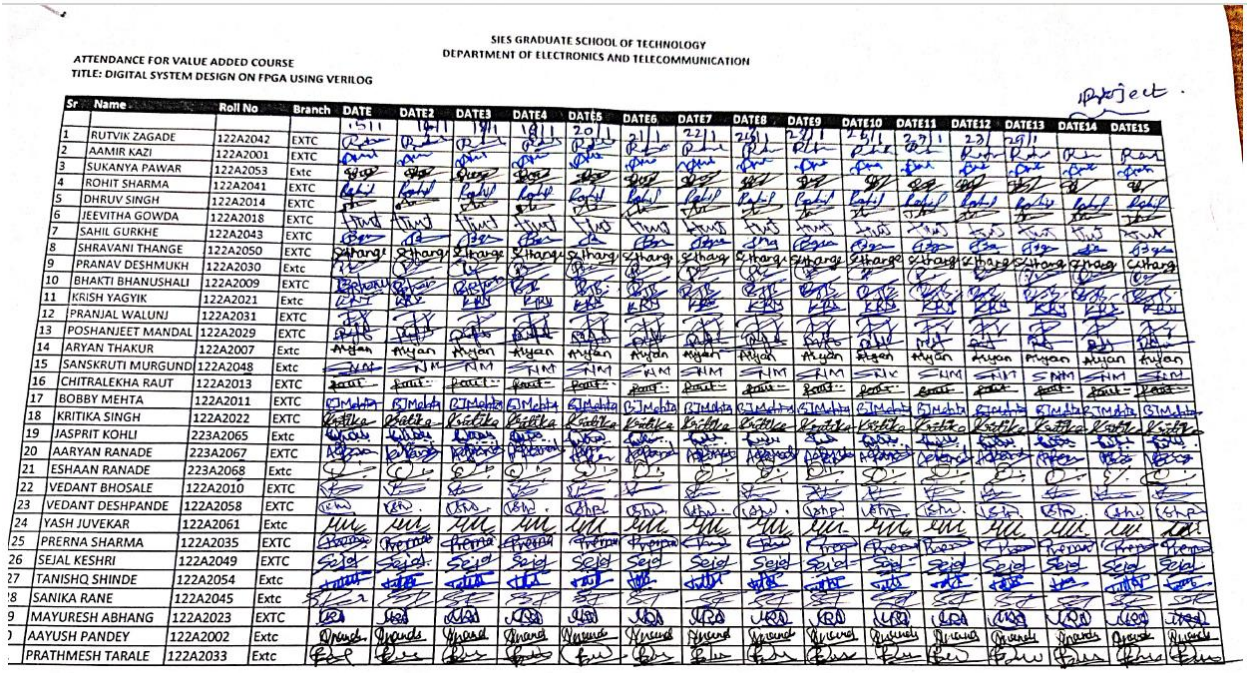
### 1. List of Students :

| Sr. No | Students name | Class | Branch | Duration Date From | Date to | Project Title |
|---|---|---|---|---|---|---|
| 1 | RUTVIK ZAGADE | TE | EXTC | 15/1/2025 | 15/2/2025 | Design of Booths multiplier using FPGA |
| 2 | AAMIR KAZI | TE | EXTC | 15/1/2025 | 15/2/2025 | Wallce tree Multiplier |
| 3 | SUKANYA PAWAR | TE | EXTC | 15/1/2025 | 15/2/2025 | Design of ALU on FPGA using verilog |
| 4 | ROHIT SHARMA | TE | EXTC | 15/1/2025 | 15/2/2025 | RISC Processor using verilog |
| 5 | DHRUV SINGH | TE | EXTC | 15/1/2025 | 15/2/2025 | RISC Processor using verilog |
| 6 | JEEVITHA GOWDA | TE | EXTC | 15/1/2025 | 15/2/2025 | FIR filter using verilog |
| 7 | SAHIL GURKHE | TE | EXTC | 15/1/2025 | 15/2/2025 | Cordic Algorithm using verilog |
| 8 | SHRAVANI THANGE | TE | EXTC | 15/1/2025 | 15/2/2025 | Timer on FPGA using Verilog |
| 9 | PRANAV DESHMUKH | TE | EXTC | 15/1/2025 | 15/2/2025 | Booths multiplier |

| | | | | | | |
|---|---|---|---|---|---|---|
| 10 | BHAKTI BHANUSHALI | TE | EXTC | 15/1/2025 | 15/2/2025 | Liecene Plate recognization using FPGA |
| 11 | KRISH YAGYIK | TE | EXTC | 15/1/2025 | 15/2/2025 | RISC Processor using verilog |
| 12 | PRANJAL | TE | EXTC | 15/1/2025 | 15/2/2025 | Liecene Plate recognization using FPGA |
| 13 | POSHANJEET MANDAL | TE | EXTC | 15/1/2025 | 15/2/2025 | Booths multiplier |
| 14 | ARYAN THAKUR | TE | EXTC | 15/1/2025 | 15/2/2025 | Wallce tree Multiplier on FPGA |
| 15 | SANSKRUTI MURGUNDE | TE | EXTC | 15/1/2025 | 15/2/2025 | Timer on FPGA using Verilog |
| 16 | CHITRALEKHA RAUT | TE | EXTC | 15/1/2025 | 15/2/2025 | Design of ALU on FPGA using verilog |
| 17 | BOBBY MEHTA | TE | EXTC | 15/1/2025 | 15/2/2025 | Huffman code generation using verilog |
| 18 | KRITIKA SINGH | TE | EXTC | 15/1/2025 | 15/2/2025 | Liecene Plate recognization using FPGA |
| 19 | JASPRIT KOHLI | TE | EXTC | 15/1/2025 | 15/2/2025 | Design of Barrial Shifter using FPGA |
| 20 | AARYAN RANADE | TE | EXTC | 15/1/2025 | 15/2/2025 | Design of Barrial Shifter using FPGA |
| 21 | ESHAAN RANADE | TE | EXTC | 15/1/2025 | 15/2/2025 | Design of Barrial Shifter using FPGA |
| 22 | VEDANT BHOSALE | TE | EXTC | 15/1/2025 | 15/2/2025 | FIR filter using verilog |
| 23 | VEDANT DESHPANDE | TE | EXTC | 15/1/2025 | 15/2/2025 | Cordic Algorithm using verilog |
| 24 | YASH JUVEKAR | TE | EXTC | 15/1/2025 | 15/2/2025 | Cordic Algorithm using verilog |
| 25 | PRERNA SHARMA | TE | EXTC | 15/1/2025 | 15/2/2025 | RISC Processor using verilog |
| 26 | SEJAL KESHRI | TE | EXTC | 15/1/2025 | 15/2/2025 | Timer on FPGA using Verilog |
| 27 | TANISHQ SHINDE | TE | EXTC | 15/1/2025 | 15/2/2025 | Image Processing on FPGA |
| 28 | SANIKA RANE | TE | EXTC | 15/1/2025 | 15/2/2025 | Image Processing on FPGA |
| 29 | MAYURESH ABHANG | TE | EXTC | 15/1/2025 | 15/2/2025 | Vedic multippiler using FPGA |
| 30 | AAYUSH PANDEY | TE | EXTC | 15/1/2025 | 15/2/2025 | 2*2 Matrix Multiplication using FPGA |

| | | | | | | |
|---|---|---|---|---|---|---|
| 31 | PRATHMESH TARALE | TE | EXTC | 15/1/2025 | 15/2/2025 | Digital Safe locker using FPGA |

## 2. Attendance report :



SIES GRADUATE SCHOOL OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

ATTENDANCE FOR VALUE ADDED COURSE
TITLE: DIGITAL SYSTEM DESIGN ON FPGA USING VERILOG

| Sr | Name | Roll No | Branch | DATE | DATE2 | DATE3 | DATE4 | DATE5 | DATE6 | DATE7 | DATE8 | DATE9 | DATE10 | DATE11 | DATE12 | DATE13 | DATE14 | DATE15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | RUTVIK ZAGADE | 122A2042 | EXTC | | | | | | | | | | | | | | | |
| 2 | AAMIR KAZI | 122A2001 | EXTC | | | | | | | | | | | | | | | |
| 3 | SUKANYA PAWAR | 122A2053 | Extc | | | | | | | | | | | | | | | |
| 4 | ROHIT SHARMA | 122A2041 | EXTC | | | | | | | | | | | | | | | |
| 5 | DHRUV SINGH | 122A2014 | EXTC | | | | | | | | | | | | | | | |
| 6 | JEEVITHA GOWDA | 122A2018 | EXTC | | | | | | | | | | | | | | | |
| 7 | SAHIL GURKHE | 122A2043 | EXTC | | | | | | | | | | | | | | | |
| 8 | SHRAVANI THANGE | 122A2050 | EXTC | | | | | | | | | | | | | | | |
| 9 | PRANAV DESHMUKH | 122A2030 | Extc | | | | | | | | | | | | | | | |
| 10 | BHAKTI BHANUSHALI | 122A2009 | EXTC | | | | | | | | | | | | | | | |
| 11 | KRISH YAGYIK | 122A2021 | Extc | | | | | | | | | | | | | | | |
| 12 | PRANJAL WALUNJ | 122A2031 | EXTC | | | | | | | | | | | | | | | |
| 13 | POSHANJEET MANDAL | 122A2029 | EXTC | | | | | | | | | | | | | | | |
| 14 | ARYAN THAKUR | 122A2007 | Extc | | | | | | | | | | | | | | | |
| 15 | SANSKRUTI MURGUND | 122A2048 | Extc | | | | | | | | | | | | | | | |
| 16 | CHITRALEKHA RAUT | 122A2013 | EXTC | | | | | | | | | | | | | | | |
| 17 | BOBBY MEHTA | 122A2011 | EXTC | | | | | | | | | | | | | | | |
| 18 | KRITIKA SINGH | 122A2022 | EXTC | | | | | | | | | | | | | | | |
| 19 | JASPRIT KOHLI | 223A2065 | Extc | | | | | | | | | | | | | | | |
| 20 | AARYAN RANADE | 223A2067 | EXTC | | | | | | | | | | | | | | | |
| 21 | ESHAAN RANADE | 223A2068 | Extc | | | | | | | | | | | | | | | |
| 22 | VEDANT BHOSALE | 122A2010 | EXTC | | | | | | | | | | | | | | | |
| 23 | VEDANT DESHPANDE | 122A2058 | EXTC | | | | | | | | | | | | | | | |
| 24 | YASH JUVEKAR | 122A2061 | Extc | | | | | | | | | | | | | | | |
| 25 | PRERNA SHARMA | 122A2035 | EXTC | | | | | | | | | | | | | | | |
| 26 | SEJAL KESHRI | 122A2049 | EXTC | | | | | | | | | | | | | | | |
| 27 | TANISHQ SHINDE | 122A2054 | Extc | | | | | | | | | | | | | | | |
| 28 | SANIKA RANE | 122A2045 | Extc | | | | | | | | | | | | | | | |
| 29 | MAYURESH ABHANG | 122A2023 | EXTC | | | | | | | | | | | | | | | |
| 30 | AAYUSH PANDEY | 122A2002 | Extc | | | | | | | | | | | | | | | |
| | PRATHMESH TARALE | 122A2033 | Extc | | | | | | | | | | | | | | | |

## 3. Feedback

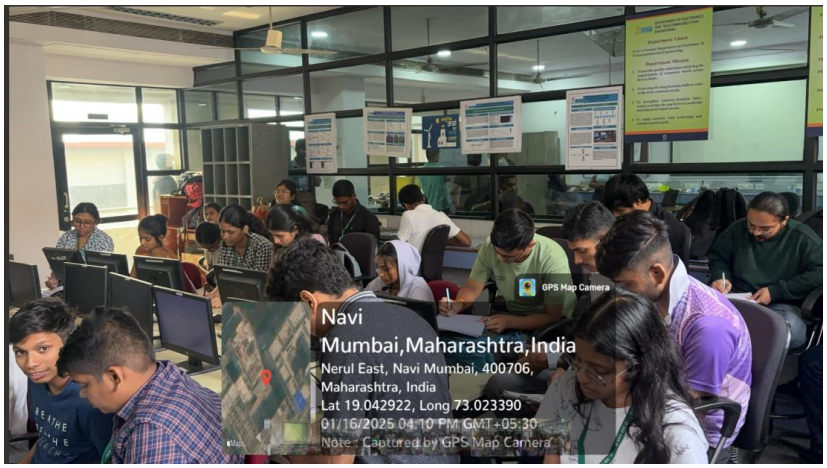
| ID | Name | Roll No | are you able to understand basic of FPGA and Verilog | Are you able to understand combinational circuit execution | Are you able to understand Sequential circuit execution? | Are you able to understand FSM execution ? | Content Delivery by Speakers | How relevant you think it was for your future | Effectiveness of SDP | Satisfaction in general | Any other suggestion or Your views about SDP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | AAMIR KAZI | 122A2001 | 5 | 4 | 5 | 4 | 4 | 4 | 5 | 5 | Nil |
| 2 | JEEVITHA GOWDA | 122A2018 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | . |
| 3 | JASPRIT KOHLI | 223A2065 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | Sdp courses are always helpful to us for all kind of projects and FPGA sdp has taught us many new and innovative things for our mini project and final year project |
| 4 | SAHIL GURKHE | 122A2043 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | No |
| 5 | SUKANYA PAWAR | 122A2053 | 4 | 4 | 4 | 3 | 4 | 4 | 5 | 3 | -- |
| 6 | BOBBY MEHTA | 122A2011 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | It was good. |
| 7 | CHITRALEKHA RAUT | 122A2013 | 5 | 4 | 4 | 4 | 5 | 5 | 5 | 5 | No |
| 8 | VEDANT BHOSALE | 122A2010 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | NA |
| 9 | ARYAN THAKUR | 122A2007 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | NO |
| 10 | AAYUSH PANDEY | 122A2002 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | No |
| 11 | DHRUV SINGH | 122A2014 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | N |
| 12 | ROHIT SHARMA | 122A2041 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | Boards are old version |
| 13 | KRISH YAGYIK | 122A2021 | 5 | 5 | 5 | 5 | 5 | 4 | 5 | 5 | None |
| 14 | YASH JUVEKAR | 122A2061 | 4 | 5 | 4 | 5 | 5 | 5 | 5 | 5 | Good course |
| 15 | SEJAL KESHRI | 122A2049 | 4 | 5 | 4 | 5 | 5 | 5 | 5 | 5 | 122A2049 |
| 16 | PRATHMESH TARALE | 122A2033 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | No |
| 17 | BHAKTI BHANUSHALI | 122A2009 | 5 | 5 | 4 | 5 | 4 | 4 | 5 | 5 | no suggestions |
| 18 | PRANJAL | 122A2031 | 4 | 5 | 4 | 5 | 4 | 5 | 4 | 5 | Na |
| 19 | RUTVIK ZAGADE | 122A2042 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | No |
| 20 | KRITIKA SINGH | 122A2022 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | None |

## 4. Certificate, Photographs (in JPEG/PNG) :

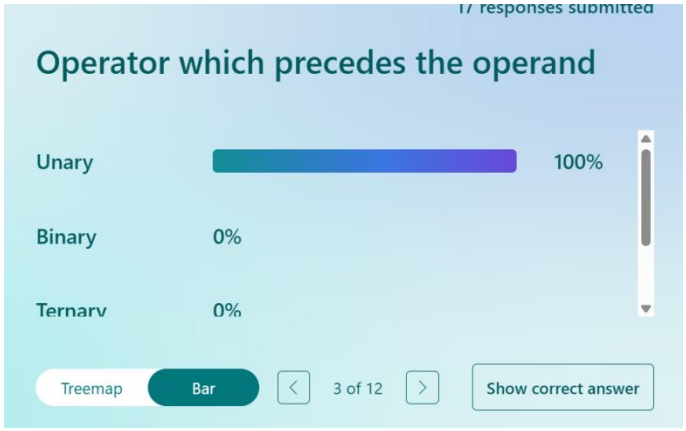

GPS Map Camera
Navi
Mumbai,Maharashtra,India
Jagatguru Aadi Shankaracharya Marg, Nerul East, Navi Mumbai, Maharashtra 400706, India
Lat 19.042453, Long 73.023046

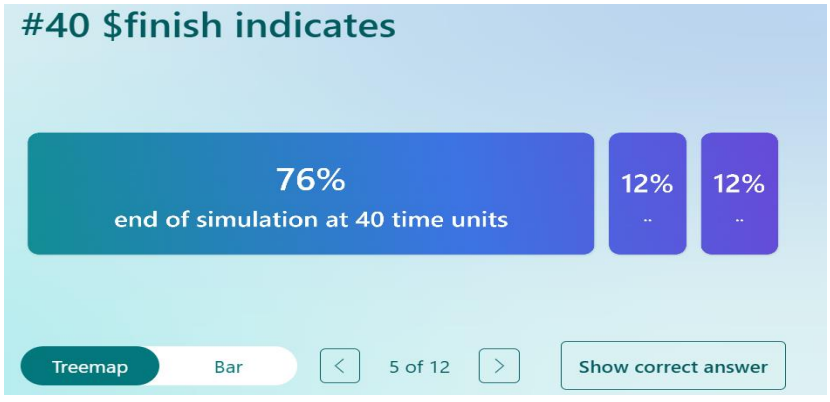

GPS Map Camera
Navi Mumbai, Maharashtra, India
Sri Chandrasekarendra Saraswati Vidyapuram Sector-v, Dr D Y Patil Vidyanagar, Sector 5, Nerul, Navi Mumbai, Maharashtra 400706, India
Lat 19.042548° Long 73.023357°
17/01/25 03:14 PM GMT +05:30
Google

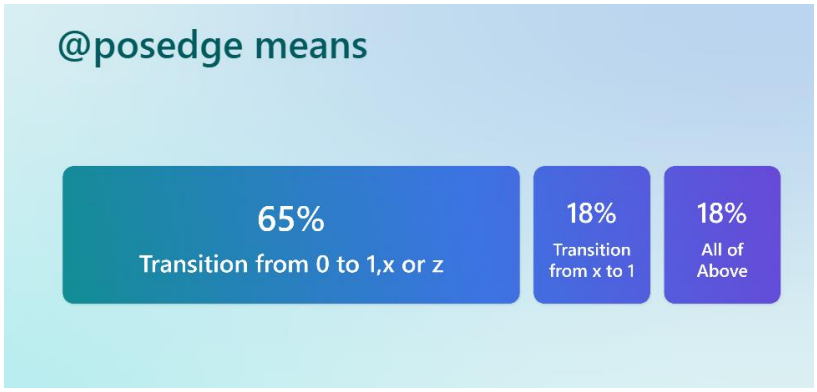

GPS Map Camera
Navi
Mumbai,Maharashtra,India
Jagatguru Aadi Shankaracharya Marg, Nerul East, Navi Mumbai, 400706, Maharashtra, India
Lat 19.042683, Long 73.022993
01/16/2025 04:10 PM GMT+05:30
Note : Captured by GPS Map Camera


GPS Map Camera
Navi
Mumbai,Maharashtra,India
Nerul East, Navi Mumbai, 400706,
Maharashtra, India
Lat 19.042922, Long 73.023390
01/16/2025 04:10 PM GMT +05:30
Note : Captured by GPS Map Camera

Quiz Result:


17 responses submitted
Operator which precedes the operand
Unary
100%
Binary
0%
Ternary
0%
Treemap
Bar
3 of 12
Show correct answer


#40 $finish indicates
76%
end of simulation at 40 time units
12%
12%
Treemap
Bar
5 of 12
Show correct answer




Certificate :