SIES Graduate School of Technology

Department of Electronics and Telecommunication Engineering

Presents

4 days Hands on Training on

FPGA Design using VHDL

December 20-22, 2017, 9.30 AM to 4.00 PM

Since their introduction in the 1985, field programmable gate arrays (FPGAs) have become increasingly important to the electronics industry. They have the potential for higher performance and lower power consumption than microprocessors and compared with ASICs, offer lower non-recurrent engineering (NRE) costs, reduced development time, easier debugging and reduced risk. Since modern FPGAs can meet many of the performance requirements of ASICs, they are being increasingly used in their place. The aim of workshop is to provide a platform for students to learn, design and implement digital system on FPGA using VHDL.

Objectives

Introduction to VLSI design flow & concepts of FPGA's & CPLD's Implementation of combinational & sequential circuits on FPGA using VHDL Design of Finite State Machine & its implementation on FPGA using VHDL

Course Contents

Introduction to VLSI design flow & concepts of FPGA's & CPLD's Combinational circuit design using VHDL & its FPGA implementation. Sequential circuit design using VHDL & its FPGA implementation. Design of Finite State Machine (FSM) using VHDL & its FPGA implementation.

Speakers

Prof. Preeti Hemnani
Prof. Preetee Khuperkar
Prof. Pranavi Mhatre
Prof. Sonal Jatkar
Prof. Priyanka Kadam

Who Should Attend

Any student from SE/TE - First come first serve (Seat available only for 20 students- 10 groups with 2 members each)

Registration Fees

Course Fees: FREE
(Cost of certificate will be applicable)

Contact for Registration

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